

Optical Interconnects for Neural and Reconfigurable VLSI Architectures

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Invited Paper

The increasing transistor density in very large-scale integrated (VLSI) circuits and the limited pin number in the off-chip communication lead to a situation described as interconnect crisis in microelectronics. Optoelectronic VLSI (OE-VLSI) circuits using short-distance optical interconnects and optoelectronic devices like microlaser, modulator, and detector arrays for optical off-chip sending and receiving offer a technology to overcome this crisis. However, in order to exploit efficiently the potential of thousands of optical off-chip interconnects, an appropriate VLSI architecture is required. We show for the example of neural and reconfigurable VLSI architectures that fine-grain architectures fulfill these requirements. An OE-VLSI circuit realization based on multiple quantum-well modulators functioning as two-dimensional (2-D) optical input/output (I/O) interface for the chip is presented. Due to the parallel optical interface, an improvement of two to three orders of magnitude in the throughput performance is possible compared to all-electronic solutions. For the optical interconnects, a planar-integrated free-space optical system has been designed leading to an optical multichip module. Such a system has been fabricated and experimentally characterized. Furthermore, we designed and manufactured fiber arrays, which will be the core element for a convenient test station for the 2-D optoelectronic I/O interface of OE-VLSI circuits.

Keywords—Associative memory, fiber arrays, neural processing, optical interconnects, optoelectronic VLSI, planar optics, reconfigurable architectures, SEED-CMOS chip, vertical-cavity surface-emitting laser (VCSEL).

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I. INTRODUCTION

The last three decades in microelectronics were determined by an enormous increase in device integration. For example, the new SUN UltraSparc III microprocessors, fabricated with 0.18- μm technology, integrate more than 16 millions transistors [1]. The end of this development is still not in sight. Unfortunately, the development of interconnects could not keep pace with advancements in transistor integration. One of the major problems in current very large-scale integrated (VLSI) systems is limited bandwidth because of too few and too slow off-chip interconnects. The imbalance between satisfying on-chip computing power and insufficient off-chip communication performance has led to a situation that is generally described as intra- and interconnect crisis in microelectronics. One of the reasons for this crisis is that off-chip interconnects are mostly located at the circuit's edge. A solution to this problem offer optoelectronic VLSI (OE-VLSI) circuits [2]. They exploit the whole chip area for communication by using a two-dimensional (2-D) optoelectronic interface to eliminate pin limitation [3]–[5]. Components for optical short-distance interconnects like microlenses, holographic optical elements, or wave-guided structures are used to link such OE-VLSI circuits optically [6]–[9]. Then data rates of several hundred gigabits/second up to 1 Tbit/s are feasible in chip-to-chip communication. This will satisfy future requirements in processor-memory and processor-processor communication. Using optics to overcome the pin limitation is also more promising than implementing three-dimensional (3-D) electronic interconnects in VLSI circuits. The possibility to stack multiple processor circuits [10], linked together by numerous optical multipoint interconnects, offers more parallelism than lots of vias between stacked metal layers in microelectronic circuits. Besides, multipoint interconnects are easier to realize with free-space optics, and much more processor arrays can be linked together.

For the success of optical short-distance interconnects between integrated circuits, it is not sufficient to focus only on

powerful optical and optoelectronic hardware. The potential of a high optical channel density will only be efficiently exploited if it is supported by an appropriate architecture. Processor architectures consisting of modules located at central processor buses will only poorly benefit from short-distance optical interconnects. In this case, data that arrive via a 2-D optical interface have to be eventually routed with long on-chip wiring to their final destination on chip. This leads also to an increase of the achievable system clock period. Hence, short-distance optical interconnects in combination with an appropriate architecture offer not only high I/O bandwidth. They avoid long on-chip interconnects too, supporting the implementation of systems with low clock period. We show in this paper that fine-grain and massively parallel architectures like neural and reconfigurable computer structures exploit the potential of optical short-distance interconnects much better.

In the past, the feasibility of microoptical components for short-distance interconnects has been demonstrated frequently. Besides, a lot of progress was also made by the development of optoelectronic devices and corresponding driver circuits to realize optical transmission and receiving directly on the chip [11], [12]. However, one of the major problems in the future is the integration of optics and electronics. Planar optical integration of free-space optics is an approach to solve this problem resulting in compact and stable systems for optical multichip modules (MCM's) [13]. In addition, fiber optical interconnects may be used for communication over longer distances (>10 cm) to connect such MCM's or packaged OE-VLSI circuits mounted on neighbored printed circuit boards. Such fiber arrays may also be used to perform specific rearrangement operations. In this paper, we present first demonstrator experiments in which a planar optical system is used for the integration of a parallel optical short-distance interconnect scheme to an OE-VLSI circuit. This circuit is based on self-electrooptical effect device (SEED) modulator technology [14]. It was fabricated through the Consortium of Optical and Optoelectronic Technologies in Computing (CO-OP) program at George Mason University sponsored by the Defense Advanced Research Projects Agency [15]. The chip realizes an optoelectronic solution for a binary neural associative memory and a reconfigurable hardware structure. Furthermore, we present results on the fabrication of fiber arrays, which we will use as primary optical part of a future test environment for OE-VLSI circuits before they are integrated in planar optical MCM's. We are reporting the results of a common interdisciplinary project among optical scientists, electrical engineers, and computer scientists.

This paper is structured as follows. In Section II, we describe the architecture model for the binary neural associative memory and explain why we selected this architecture for a realization. We will discuss the background of neural processing in this context and then focus on optoelectronic technology. In Section III, we theoretically derive the throughput performance of the optoelectronic solution and compare it to pure electronic systems. Section IV focuses on the hardware realization. This includes three aspects: design and test of the OE-VLSI chip and the optical interconnects and the integration of both. We conclude our results in Section V.

II. APPROPRIATE VLSI ARCHITECTURES FOR SHORT-DISTANCE OPTICAL INTERCONNECTS

Due to their inherently irregular architecture, traditional von Neumann structures are not suited to benefit significantly from highly dense optical chip-to-chip interconnections. Architectures that exploit optical interconnections efficiently have to take into account the locality and regularity of optical imaging systems [16]–[18]. Examples for architectures that fulfill these conditions are neural and reconfigurable computing structures [19]–[21]. Although neural architectures are not going to be the mainstream architectures in the future, they exhibit certain features that will be found in more general-purpose architectures like massively parallel computer systems too. These are large fan-in and fanout, large portion of global interconnects within the chip area, and a parallel memory access. In particular, such interconnect schemes are well suited to be realized by 3-D optical interconnects. This allows one to exploit large chip areas for logic circuitry that are wasted for wiring otherwise. Furthermore, neural structures are well suited for experiments demonstrating the benefits of optoelectronic interconnection topology. First, we explain in this subsection in more detail why the computing performance of traditional von Neumann architectures will not improve by using short-distance optical interconnects. Afterwards, we present the architecture model of a binary neural associative memory we selected for implementation with optoelectronic technology.

A. Short-Distance Optical Interconnects and General-Purpose Microprocessors

Currently, the architecture setup of most microprocessors resembles strongly the traditional von Neumann principle. Functional units like the control, integer and floating-point unit form a central processing unit (CPU). In the past, the CPU was expanded by more and more memory units like cache and memory management components to diminish the von Neumann bottleneck [22]. But as usual in von Neumann architectures, all functional units are still grouped around a central processor bus. Furthermore, as Fig. 1 shows, a modem microprocessor like the Intel Pentium consists of a variety of modules, like, e.g., the memory management unit, the control unit, and the cache. As illustrated, the number of data bits which are exchanged between those modules on-chip via a central processor bus is varying considerably.

The data path width between control and integer unit on one side and the cache on the other side is 320 bits. Whereas the memory management unit and the cache transfer only 96 bits among each other, the floating-point unit needs in a closer distance an internal bus width of 80 bits. This geometrically irregular distribution of on-chip data traffic is in a certain contrast to the regular setup of arrays of microlasers, modulators, or microlenses, which are needed to realize short-distance optical interconnects. As a result, incoming optical input data must be routed with long running wires on an additional metal layer to the final destination on the chip after electrical–optical conversion. A similar situation is given for optical interchip interconnects. In this

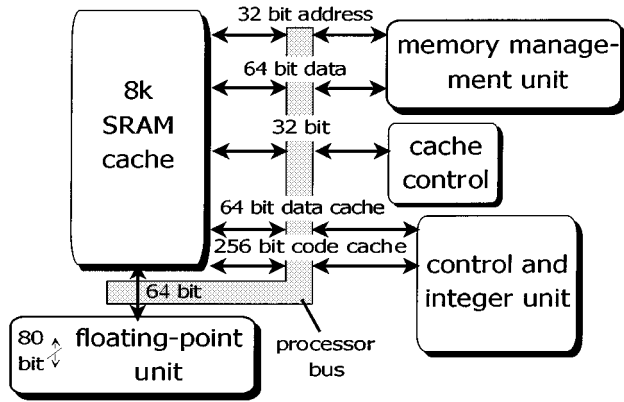


Fig. 1. Data flow in a von Neumann architecture. Simplified representation of the block diagram in [23].

case, external interconnects located at the circuit's edge will be replaced by a 2-D array of optoelectronic interconnects, enlarging the number of possible off-chip connections. But again, an irregular data traffic is given because different functional units show different strong data requirements to the chip's outside world.

A more efficient use of short-distance optical interconnects than in von Neumann architectures is guaranteed if the architecture consists of fine-grained, massively parallel architectures [24], [25] with tens to hundreds of thousands of simple processing elements (PE's) on one chip. Then the high space bandwidth of optical interconnects is exploited best. Furthermore, stacked and optically linked circuit planes [10] allow one to realize 3-D architectures with pipeline processing in superpipelined and superscalar units.

B. Efficient OE-VLSI Architectures Using Short-Distance Optical Interconnects

The first example of an architecture we selected for a realization with existing OE-VLSI circuit technology is a binary neural associative memory. This architecture was proposed by Palm [26]. It has a series of features that are ideally appropriate for a solution with optical interconnects, as recognized by other groups, too. In [27], a solution for such an architecture based on liquid crystal technology is presented. Our solution uses OE-VLSI circuits and a planar optical system [13] to realize fast operation and compact integration. To understand better the benefits of such an architecture for an optoelectronic solution, we first explain the functionality of the architecture.

As usual in an associative memory, we are using a key vector y to read out a vector x , which was stored before in the associative memory (see Figs. 2 and 3). In addition, in a binary associative memory, all components of the vectors as well as the content of a single associative memory cell have either the value 1 or 0. All memory cells are arranged in a matrix with components w_{ij} . During a learning cycle, the content of w_{ij} is determined as the logical sum of AND opera-

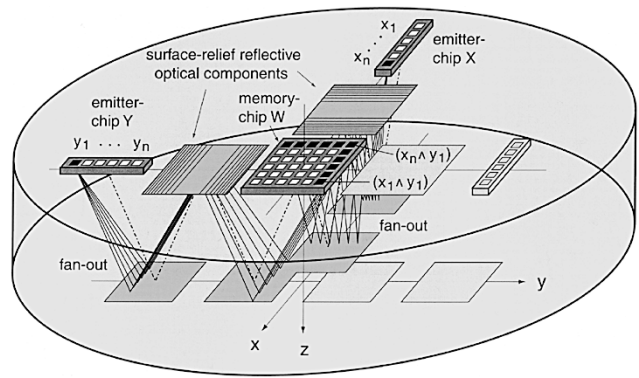


Fig. 2. Parallel optical data flow to the optoelectronic associative memory module during the learning cycle (1).

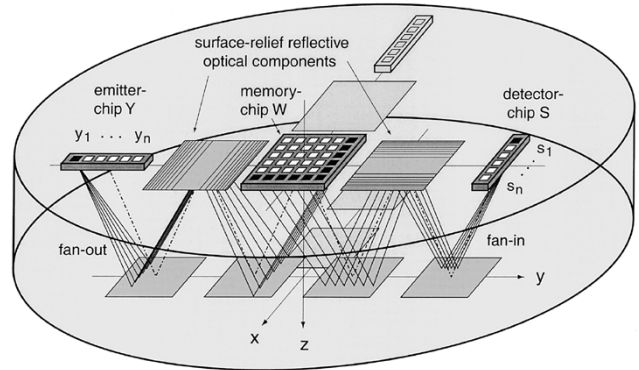


Fig. 3. Parallel optical data flow to the optoelectronic associative memory module during the recognition cycle (2).

tions between the j th component of y and the i th component of x for all m vector pairs (x, y) we want to store (1)

$$\begin{aligned}
 w_{ij} &= \bigvee_m (x_i^{(m)} \wedge y_j^{(m)}) \\
 &= (x_i^{(1)} \wedge y_j^{(1)} \vee \dots \vee x_i^{(m)} \wedge y_j^{(m)}) \\
 \wedge &: \text{logical AND} \\
 \vee &: \text{logical OR}
 \end{aligned} \tag{1}$$

During readout, i.e., in the recognition cycle, a vector matrix product of the input vector y with the matrix of associative memory cells w_{ij} is carried out and a subsequent threshold operation ($\geq \theta$) is applied to the result to determine the components of the output vector s (2). Because the values are all binary, the multiplication is reduced to count logical 1's along columns in that rows i , where the i th component of y is equal to one. Furthermore, the parallel addressing scheme of such an associative memory can be fully supported using 3-D optical interconnect technology

$$s_i = \begin{cases} 1, & \text{if } \sum_j (y_j \wedge w_{ij}) \geq \theta \\ 0, & \text{else.} \end{cases} \tag{2}$$

The implementation we propose is sketched in Figs. 2 and 3. A planar-integrated free-space optical system, which consists of surface-relief reflective optical components, interconnects four optoelectronic components that are mounted on it; the 2-D OE-VLSI-memory-array W , the two 1-D ver-

tical-cavity surface-emitting laser (VCSEL) arrays X and Y , and the 1-D photodiode-detector array S represent matrix W and vectors x , y , and s , respectively. For the learning step shown in Fig. 2, the highlighted components X , Y , and W are involved. Binary signals from both emitter arrays are fanned out in one direction by the optical system and superimposed on the memory array. Through a binary detection with an appropriately adjusted threshold, the optoelectronic memory cells generate and store the result of (1). To obtain w_{ij} according to (1), this process needs to be repeated for all m vector pairs; the memory contents of each cell is thereby updated after each step using a logical OR-operation. The readout (see Fig. 3) involves components Y , W , and S . Signals representing a key vector y are fanned out in one direction and address the modulator elements of the memory cells, which are either in the high- or in the low-reflectivity state depending on the respective memory content. The modulated signals are then fanned in the orthogonal direction and superimposed at the detector elements. A threshold operation, realized by an adjustable electronic comparator, completes the implementation of (2).

Besides this neural structure, a parallel optical access to a chip is also very attractive for reconfigurable hardware. There the functionality is programmed by loading a bitstream in lookup tables as, for example, in field-programmable gate arrays (FPGA's) [28]. Due to a possible parallel optical access, this loading can be carried out dynamically and in different circuit parts very fast, which is only difficult to realize in pure electronics. Therefore, we decided to also implement optoelectronic reconfigurable hardware on our test chip. For the test chip, we programmed the lookup tables as associative memory cells. This simplifies the integration of two different architectures in one test environment.

III. PERFORMANCE IMPROVEMENT OF OPTOELECTRONIC VERSUS PURE ELECTRONIC ARCHITECTURES

To estimate to first order the possible performance gain for the optoelectronic associative memory, we have to calculate the number of connections that can be switched in one second. This is expressed in giga connections per second (GCPS), the figure of merit to measure the performance P in neural architectures. This figure is equal to the number of memory cells we can address in parallel. The number of memory cells we can integrate is determined by the quotient of chip size A_{Chip} , and the area A_{PE} , needed for one memory cell. This ratio multiplied with the clock frequency f results in the number of switchable links per second (3). A_{PE} is determined by the number of necessary transistors N_{Trans} in the PE multiplied with the reciprocal of the transistor integration density I_{Trans} for a specific technology. Furthermore, it must hold that the optical pitch may not be too small because otherwise the PE does not fit in the area defined by the raster of the optical input/output pads. That means that A_{PE} is upper limited by the area A_{Opto} needed for the 2-D optoelectronic off-chip interface in each PE, i.e., it must hold that $A_{\text{PE}} \leq A_{\text{Opto}}$. A_{Opto} depends on the pixel raster $N_x \times N_y$ and the pitch size p_x and p_y of the optical input/output de-

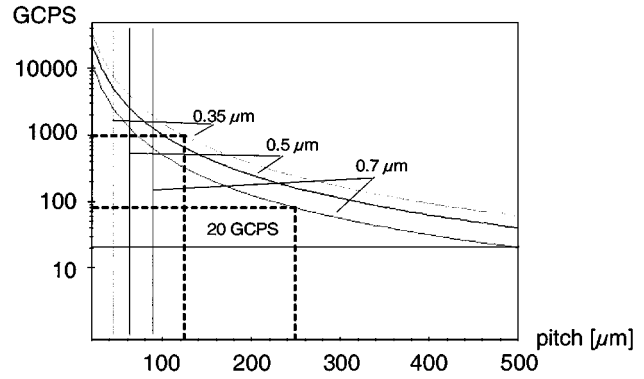


Fig. 4. Performance evaluation for the optoelectronic binary neural associative memory.

vices one PE needs in x - and y -direction. For our binary neural associative memory, we need one optical input and output. Hence the pixel raster can be 2×1 . Fig. 4 shows the maximum performance P versus pitch size

$$P = \#PE's \cdot f = \frac{A_{\text{Chip}}}{A_{\text{PE}}} f = \frac{A_{\text{Chip}}}{1/I_{\text{Trans}} \cdot N_{\text{Trans}}} \leq \frac{A_{\text{Chip}}}{N_x \cdot N_y \cdot p_x \cdot p_y} f = \frac{A_{\text{Chip}}}{A_{\text{Opto}}} f. \quad (3)$$

We assumed an identical pitch size p in x - and y -direction, a chip area A_{Chip} of 1 cm^2 , clock frequencies f of 100, 200, and 300 MHz, and transistor integration densities of $1 \cdot 10^6$, $2 \cdot 10^6$, and $3 \cdot 10^6$ transistors/ cm^2 , as they are specified in the SIA roadmap [29] for different minimum structure sizes. We needed 79 transistors for the integration of one memory cell. This figure allows us to calculate the lower limit for the pitch size, i.e., the situation where A_{Opto} is smaller than A_{PE} . The vertical lines on the right side in Fig. 4 show these limits. The horizontal line in Fig. 4 running at 20 GCPS corresponds to the performance of a purely electronic system [30]. We see that for reasonable pitch sizes between 125 and 250 μm , our optoelectronic solution allows an improvement of up to two magnitudes. Even if the purely electronic system is some years old now, we must consider that the electronic system was distributed on 16 printed circuit boards, whereas the performance lines in Fig. 4 in the optoelectronic case hold for one single optoelectronic chip.

IV. HARDWARE REALIZATION

Due to the impressive performance increase we can achieve with an optoelectronic solution, we decided to realize this architecture with a first demonstrator chip and a corresponding optical MCM based on planar optics. To limit the costs for that demonstrator, we restricted ourselves to an associative memory array of size 8×10 . After arranging the interfaces between optics and electronics, the optical and optoelectronic part of our system were designed separately as well as the fiber array we wanted to use as a test system for OE-VLSI chips. First we describe the OE-VLSI chip and the fiber array. Then we explain in detail the setup and realization of the planar optical system.

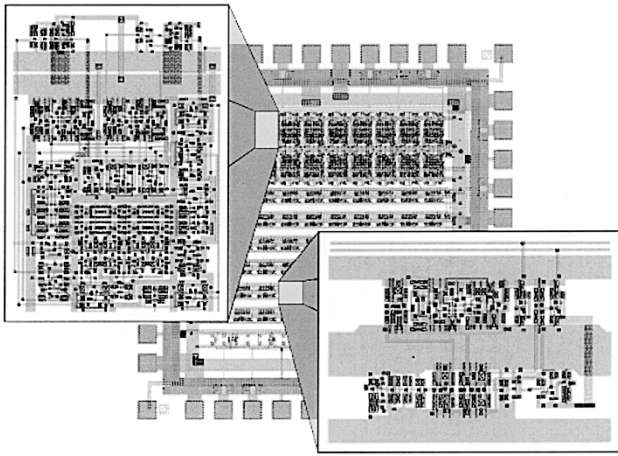


Fig. 5. Physical VLSI layout of the SEED-CMOS chip.

A. Design and Test of Optoelectronic VLSI Chip

The architecture was realized in a first demonstrator chip by using hybrid SEED-CMOS technology [14]. It became available through a multiproject wafer run organized by CO-OP. In this technology, optical inputs and outputs are provided using SEED diodes. These GaAs devices are flip-chip bonded on top of the silicon and electrically connected to the third metal layer. SEED devices can work as photodiodes as well as optical reflection modulators. They are arranged in a fixed array raster of 20×10 within a tiny chip of 1.2-mm edge length. This corresponds to a pitch of $62.5 \mu\text{m}$ horizontally and $125 \mu\text{m}$ vertically. We carried out a full custom design of the chip. The result is shown in Fig. 5 without the third metal layer, in which the electronic interconnects to the SEED diodes are realized.

The CMOS circuit was fabricated by a HP-CMOS14TB process with $0.5\text{-}\mu\text{m}$ technology through the metal-oxide semiconductor implementation service (MOSIS). The magnification on the lower right corner shown in the physical layout of Fig. 5 corresponds to one single associative memory cell. There are 60 of those smart pixel cells on the test chip. Each cell contains only 79 transistors. The extracted layout was successfully simulated in SPICE up to 166 MHz. With a dual-rail coding scheme, in which two SEED diodes are used in reverse mode to code 1 and 0, we could simulate an access time of 4 ns. However, we decided on a single-rail coding because we did not want to lose space bandwidth.

In the left rectangle of Fig. 5, the VLSI layout of one cell of the reconfigurable hardware structure is shown. Reconfigurable hardware is also very attractive for optical interconnects because the parallel optical access to a circuit allows a fast dynamic and partial reconfiguration of programmable hardware. Therefore, we implemented on the chip 20 optically addressable lookup tables of size 4×2 . They are shown in the middle of the closeup of the chip in Fig. 6. Due to the parallel optical access to the lookup tables, they all can be reconfigured in microseconds as we verified by SPICE simulations. In comparison, the reconfiguring of lookup tables in

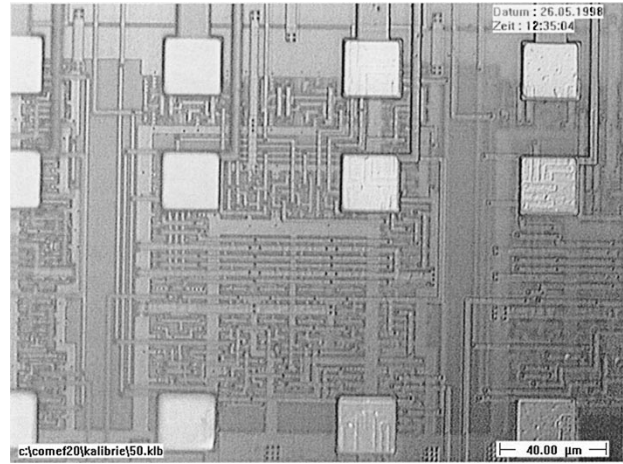


Fig. 6. Closeup of the chip. The rectangular metallic bond areas are the contact pads for the SEED modulators.

FPGA devices needs milliseconds. Hence, our optoelectronic solution allows an improvement of about three magnitudes.

For comparison purposes, we also designed for the binary neural associative memory a purely electronic chip using standard cell techniques for a $0.5\text{-}\mu\text{m}$ CMOS technology. As the most obvious advantage, the optoelectronic solution results in significant chip area savings of about 50%. That means, in the optoelectronic solution we can use twice the chip area for the implementation of logic circuitry. In the purely electronic system, much chip area is lost for the required on-chip wiring of the global signals. These results are valid for a 10×10 array, which requires 20 global data signals. Larger arrays require still more global signals and will result in still better area savings for the optoelectronic solution. This holds due to the more than linear increase in chip area necessary for implementing global signals. Free-space optical interconnects allow one to implement global interconnects through free space with minimum on-chip signal routing. Thus long interconnects on the chip are eliminated since data are directly transferred to the desired chip location.

B. Fiber-Array-Based Test Station

To carry out measurements determining the contrast ratio and the wavelength sensitivity of the SEED modulators, a fiber-based test environment was designed. The main part of the fiber-based test station is a fiber array that allows one to address a large part of the 2-D optical input/output interface of the chip simultaneously. To realize that, components were developed for an optical fiber-based coupling of emitter and receiver to the optical associative memory chip [31]. This included the development of a new technology for the manufacturing of 2-D fiber arrays with pitch sizes of 500 and $250 \mu\text{m}$ [32]. Similar work had been carried out in the United States [33], Japan [34], [35], and Germany [36]. Fig. 7 schematically displays the manufacturing process. The holes, in which multimode fibers are mounted in a specified configuration, were etched in a silicon wafer. By means of hybrid

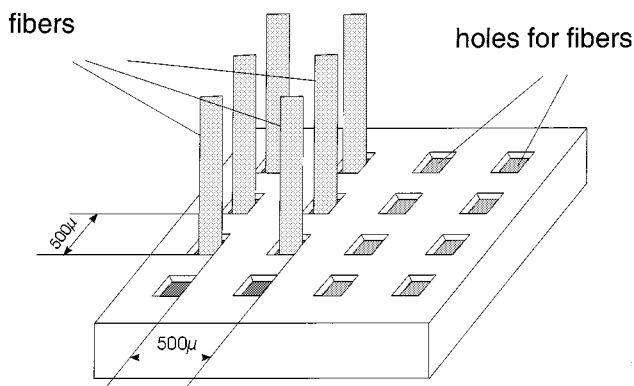


Fig. 7. Fiber array with conic etched holes.

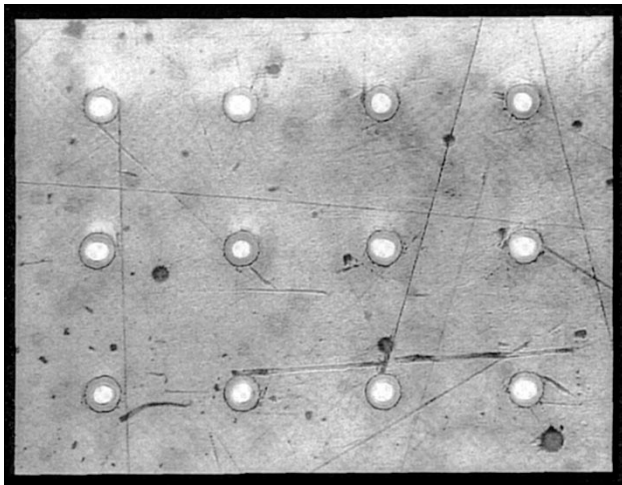


Fig. 8. A 2-D multimode fiber array with 500- μ m pitch.

integration and micromounting techniques, the fibers were fixed in well-defined height and distance. We produced 5×5 and 4×4 imaging fibers with a pitch accuracy better than $5 \mu\text{m}$. A total channel number of about 30 has been demonstrated. The number of fibers can be easily extended to 100 and more. Fig. 8 shows the front side of a fiber array with 500- μ m pitch. The fibers are illuminated from the rear. The brighter part of the fiber shows the core. For this particular array, we achieved an accuracy below $5 \mu\text{m}$ for the pitch size, absorption differences between the fibers were below 7%, and a crosstalk was not measurable. The technology allows us also to arrange the fibers at both ends of the array in a different pattern. As an example, a perfect shuffle operation has been realized in two dimensions. By this way, specific processing operations can be incorporated in the 2-D fiber structure.

In order to achieve a pitch of $125 \mu\text{m}$, we have performed experiments to develop an appropriate manufacturing technology. Such an array will allow us to control directly the 2-D optoelectronic interface of the SEED chip in the future. So far, to test single SEED elements, we used a simpler test setup to carry out first experiments. The main part of this test setup is a fiber-based X-coupler (see Fig. 9). The emitted light of a laser source is coupled into one branch at the left side of this X-coupler. The reflected light by the SEED modulator is sent back to the other branch of the X-coupler at the

left side and measured by a photo detector. One branch at the right side of the X-coupler is directly positioned above the SEED modulator. The other branch is used for monitoring the output wavelength.

To get a prediction about the required positioning accuracy, we have varied the position of that fiber branch directly positioned over the SEED element. We have determined that an accuracy of $5 \mu\text{m}$ is sufficient to carry out a reliable digital data communication. For the SEED multiple quantum-well diodes, a responsivity of about 0.45 A/W has been determined. At the moment, we carry out tests to detect the critical frequency, the wavelength dependence of the SEED elements, and the contrast ratio. Unfortunately, the SEED elements show a strong wavelength dependency. At a wavelength of 844 nm, we determined a contrast ratio of about 4.5%. To get better results, the output wavelength of the laser was analyzed and tuned between 845 and 855 nm. By choosing an optimized wavelength, an improvement by a factor of three has been observed. This was sufficient to verify the principle operation capability of a memory cell. Unfortunately, the measured access times were only 60 MHz so far. It is very difficult to realize a high-performance setup using the sensitive SEED technology. We think much better results can be achieved if we use an optoelectronic chip with VCSEL's as light output source. Regrettably, VCSEL's were not available for us when we started the project. VCSEL's offer a high output power ($>1 \text{ mW}$) and a fast modulation time ($>1 \text{ GHz}$). Furthermore, the optical setup is simplified because no additional external light source is necessary. Using detectors that are monolithically integrated with silicon electronics, it is possible to receive light pulses with a rate up to 1 Gb/s [37]. Such a setup would not show this wavelength dependency, as it is the case for SEED modulators. An OE-VLSI technology based on VCSEL's offers so much potential that the simulation result of 166 MHz should be experimentally verified without problems. Nevertheless, the experience we gained in designing a microoptical setup and an OE-VLSI chip so far by using the modulator technology is valuable and will help us if we exploit VCSEL technology in the future.

C. Planar Optical Interconnection Scheme

The concept of planar optics as illustrated in Figs. 2 and 3 combines the potential of free-space optical systems in implementing complex and fully 3-D interconnects with the benefits of device integration to obtain compact, stable, and potentially cheap systems. An optical system is "folded" into a planar transparent substrate in a way so that functional optical components are located at the surfaces. Since the system is fabricated as a whole, fabrication complexity does not depend on the complexity of the optical system. Hence, unlike in a discrete optomechanic interconnect setup, a sophisticated system design that can efficiently suppress crosstalk does not increase production cost.

The interconnection scheme of the associative memory consists of the basic operations fanout and fan-in. For implementing these operations, we employed what is known under the term hybrid optical design concept: Arrays of microele-

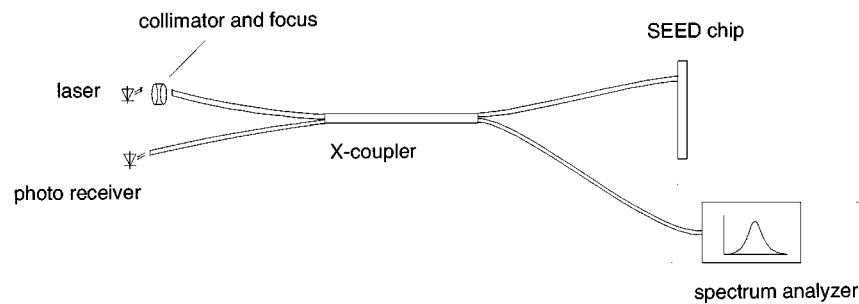


Fig. 9. Setup for simple measurements of single SEED elements.

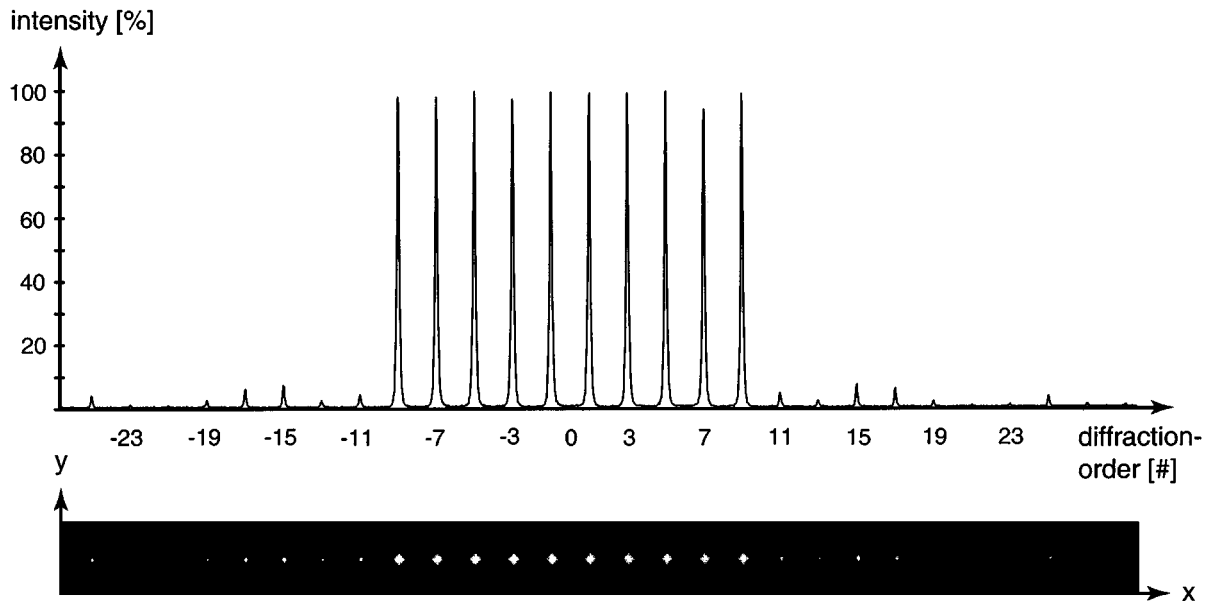


Fig. 10. Diffraction pattern generated by the fanout DOE.

ments with local effect and individual elements with global effect are combined [38]. This approach provides a large number of adjustable parameters, which are used to eliminate or balance optical aberrations [6]. It is particularly well suited when distinct parts of a continuous field like the OE-interfaces on VLSI-chips are to be interconnected. In order to concentrate the energy on the SEED elements, we have designed a fanout system, which contains an array illuminator (AI) [39]. AI's are diffraction gratings, which distribute the energy of an incoming plane wave equally into a certain number of predetermined diffraction orders. In our case, an AI with a symmetric linear fanout of ten is needed. For the design, we used an iterative Fourier transformation algorithm (IFTA), also known as a Gerchberg–Saxton-type algorithm [40]. To avoid absorption losses, we required the grating to be phase only. With such an AI, we obtained experimentally the diffraction pattern of Fig. 10. Obviously, the energy is almost completely (theoretical efficiency limit 95.3%) and very uniformly (mean deviation $< 2\%$) distributed among ten equally spaced diffraction orders.

The above considerations lead to a system design for the interconnects of the associative memory as depicted in [41] and [42]. Note that the interconnection of emitter array X and memory array W is identical to the one between Y and W and therefore not explicitly shown here. To facilitate

fabrication, we designed the system so that all surface-relief optical structures lie on one surface of the substrate. The four chips X , Y , W , and S are to be mounted on a separate $500\text{-}\mu\text{m}$ -thick transparent substrate to provide the necessary spacing between the OE-interfaces and the corresponding microlens arrays. Inside the planar substrate, each signal bounces four times between the two surfaces to get from one chip to the next. In the y - z cross section of Fig. 11, the system performs an imaging in the left part and a collimation in the right part. In the orthogonal cross section, it is a multiple beam splitting by the AI and an imaging, respectively. The phase functions of AI and the field lens of the hybrid imaging system on the left have been combined to yield one single diffractive optical element, which we refer to as fanout DOE.

The optical system has been fabricated using a binary two-mask lithographic and a reactive ion etch process, providing a surface relief with four equally spaced levels. This technique guarantees submicrometer alignment accuracy and very high functional precision. The reflective components have been coated with a thin layer of aluminum. We fabricated the top and bottom side of the system on two separate 3-mm-thick substrates, which were then cemented together. Fig. 12 shows a photograph of the top-side part before cementation. The reflective, coated and

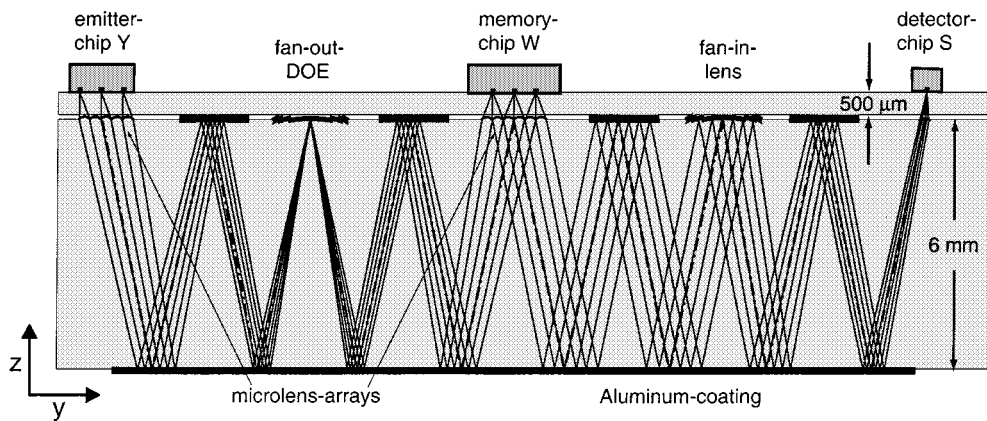


Fig. 11. Cross section of the planar optical interconnection scheme.

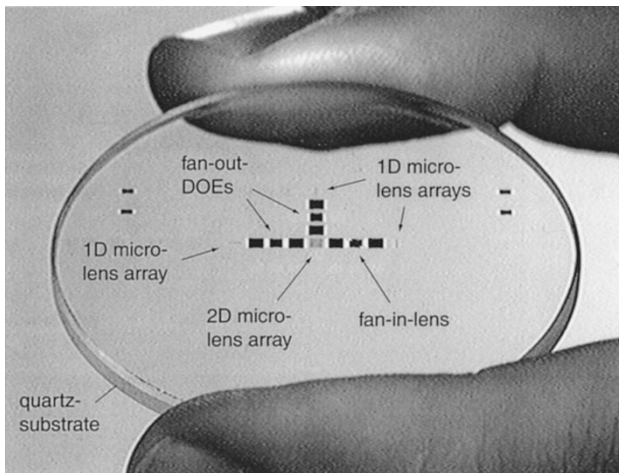


Fig. 12. Top-side part of the planar-optical system.

the transmissive, uncoated components are clearly visible in two different gray shades. The optical performance of the system has been tested experimentally. Thanks to the hybrid approach, we obtained a very uniform and nearly diffraction-limited imaging quality over the whole field.

Fig. 13 shows part of the central microlens array together with the signal spots generated by the microlenses at the memory chip. From the intensity plot across the center of such a signal spot, it is obvious that the SEED elements with an area of $20 \times 20 \mu\text{m}^2$ can easily cover the whole signal.

V. CONCLUSION

In this project, we demonstrated an optoelectronic system using VLSI technology and integrated free-space optics. Such systems have the potential to form the basis for future implementations of massively parallel computers, which allow much more throughput performance than pure electronic solutions. Exploiting efficiently the potential of short-distance optical interconnects requires a well-suited architecture that is well adapted to the boundary conditions given by optical and optoelectronic hardware. We pointed out that traditional von Neumann architectures are not appropriate in this context. Much more efficient are fine-grain, single-instruction multiple-data-like architectures, which

exploit efficiently the high interconnect density optics provides. As architecture examples, we selected for the realization a binary neural associative memory and a reconfigurable hardware. In a theoretical analysis, we showed that a single OE-VLSI circuit of 1 cm^2 size offers up to two times more performance than an existing pure electronic solution realized on 16 printed circuit boards a few years ago. The OE-VLSI circuit was designed on layout level and manufactured via a multiple wafer run organized by CO-OP, DARPA, and Lucent. The chip uses SEED devices as optoelectronic interface for the chip-to-chip communication. Optically addressable lookup tables were implemented on the chip as well. SPICE simulations result in an access time of at least 166 MHz. Due to the parallel access by optical interconnects, this corresponds to an improvement of three magnitudes over the reconfiguration time in electronically reconfigurable hardware.

Furthermore, we developed and designed a new technology for the manufacturing of fiber arrays, which will be the main part in a pluggable fiber-based smart pixel test station. The advantage of such a system is the possibility to test comfortably a large part of the 2-D optoelectronic interface of an OE-VLSI chip. Besides, such fiber arrays can also be used for the realization of highly dense short-distance optical interconnects between closely neighboring printed circuit boards, i.e., to connect a memory card with a processor card with more than 1000 links. So far, fiber arrays in silicon with a pitch size of 250 and $500 \mu\text{m}$ and an array size of 4×4 and 5×5 were manufactured by etch processes, hybrid integration, and micromounting techniques. We measured an accuracy below $5 \mu\text{m}$ for the pitch size, the absorption differences between the fibers were below 7%, and no crosstalk was detectable. The next step is the coupling of the fiber array with the OE-VLSI chip. So far, the principal functionality of the optical I/O pads was proved with a X-coupler system, in which input and output signals were observed in different branches of the coupler.

For shorter distances over the range of few centimeters, free-space optics is preferable to connect OE-VLSI circuits. We used a planar optical integration of free-space optics that results in compact and stable systems for optoelectronic MCM's. Thus the optics is fabricated with the same

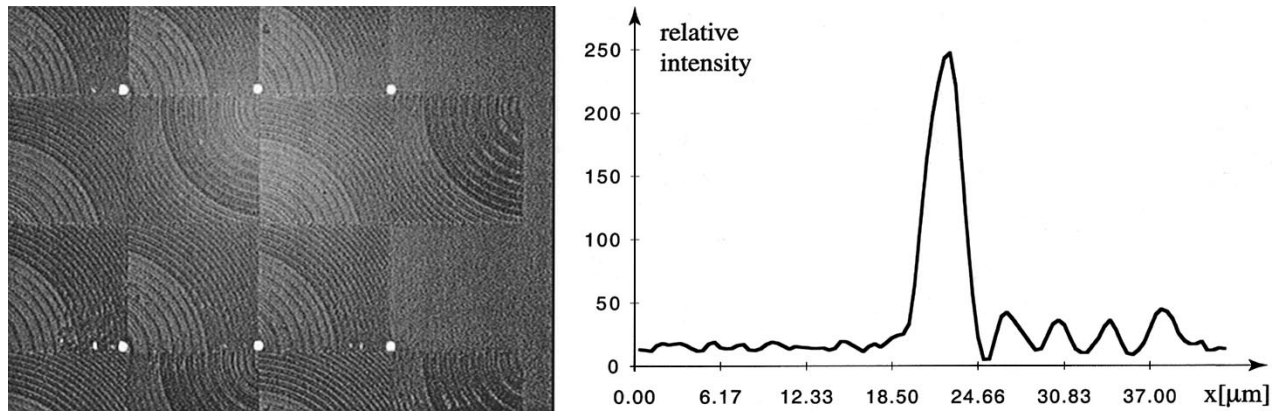


Fig. 13. Part of the central microlens array and signal spots generated by the microlenses at the memory chip.

lithographic fabrication technology that forms the technological platform for optoelectronic integration. In such a planar optics scheme, our OE-VLSI chip will be integrated with optical fanout interconnects of two one-dimensional VCSEL arrays. Furthermore, the optical output of the chip is collected with an optical fan-in element. To realize the fanout for our optoelectronic prototype system, diffractive phase gratings with a fanout of ten were designed by an iterative Fourier transform algorithm. We verified experimentally a high uniformity in the ten diffraction orders, and the mean deviation was below 2%. We achieved a high diffraction intensity as well. This almost reaches the theoretical limit of 95%. The main reason for this satisfying result is the hybrid approach we pursued in the design of the optical imaging system. That means the fanout and fan-in interconnects are realized with a setup consisting of a microlens array and a collection macrolens, which is the ideal approach for illuminating dilute arrays. The optical system was fabricated using a binary two-mask-lithographic and a reactive ion etch process. This technique guarantees submicrometer alignment accuracy and very high functional precision demonstrating a viable technology approach for optoelectronic MCM's. The microoptical setup is now ready for the integration of the OE-VLSI chip, which will be the next step of our work.

REFERENCES

- [1] R. Cook, "Chips are always harder to design than roadmaps," *SUN World*, Nov. 1998.
- [2] J. W. Goodman, F. J. Leonberger, S. Kung, and R. A. Athale, "Optical interconnections for VLSI systems," *Proc. IEEE*, vol. 72, pp. 850–865, 1984.
- [3] Y. Liu, E. M. Strzelecka, J. Nohava, M. K. Hibbs-Brenner, and E. Towe, "Smart-pixel array technology for free-space optical interconnects," *Proc. IEEE*, vol. 88, pp. 764–768, June 2000.
- [4] A. V. Krishnamoorthy, L. M. F. Chirovsky, W. S. Hobson, R. E. Leibenguth, S. P. Hui, G. J. Zydyk, K. W. Goosen, J. D. Wynn, B. J. Tseng, J. A. Walker, J. E. Cunningham, and L. A. D'Asaro, "Vertical cavity surface-emitting lasers flip-chip bonded to gigabit-per-second CMOS circuits," *IEEE Photon. Technol. Lett.*, vol. 11, no. 1, pp. 128–130, 1999.
- [5] J. Jahns, "Free-space optical digital computing and interconnection," *Progress Opt.*, vol. 38, pp. 419–513, 1998.
- [6] S. Sinzinger and J. Jahns, "Integrated microoptical imaging systems with high interconnection capacity fabricated in planar optics," *Appl. Opt.*, vol. 36, pp. 4729–4735, 1997.
- [7] J. Bähr and K.-H. Brenner, "Optical motherboard: A planar chip-to-chip interconnection scheme for dense optical wiring," in *Proc. Optics in Computing OC'98*, Brugge, June 1998, pp. 419–422.
- [8] M. R. Feldman, "Holographic optical interconnects for multichip modules," *Proc. SPIE*, vol. 1390, pp. 427–433, 1990.
- [9] R. T. Chen, L. Lin, C. Choi, Y. J. Liu, B. Bihari, L. Wu, S. Tang, R. Wickmann, B. Picor, M. Hibbs-Brenner, J. Bristow, and Y. S. Liu, "Fully embedded board-level guided-wave optoelectronic interconnects," *Proc. IEEE*, vol. 88, pp. 780–793, June 2000.
- [10] P. J. Marchard, X. Zhueng, D. Huang, O. Kibar, and S. C. Esener, "Free-space optical interconnects for multi-chip environment," *Proc. IEEE*, to be published.
- [11] M. Kuijk, D. Coppee, and R. Vounckx, "Spatially modulated light detector in CMOS with sense-amplifier receiver operating at 180 Mb/s for optical data link applications and parallel optical interconnects between chips," *IEEE J. Select. Topics Quantum Electron.*, vol. 4, pp. 1040–1045, Nov./Dec. 1998.
- [12] F. E. Kiamilev, "500-Mb/s 32-channel CMOS VCSEL driver with built-in self-test and clock generation circuitry," *Proc SPIE Optoelectronic Integrated Circuits and Packaging III*, vol. 363, pp. 18–26, 1999.
- [13] J. Jahns, "Planar packaging of free-space optical interconnections," *Proc. IEEE*, vol. 82, pp. 1623–1631, 1994.
- [14] A. V. Krishnamoorthy, A. L. Lentine, K. W. Goosen, J. A. Walker, T. K. Woodward, J. E. Ford, G. F. Aplin, L. A. D'Asaro, S. P. Hui, and B. Tseng, "3-D integration of MQW modulators over active sub-micron CMOS circuits: 375 Mb/s transimpedance receiver-transmitter circuit," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1288–1290, 1995.
- [15] A. V. Krishnamoorthy and K. W. Goosen, "Progress in optoelectronic-VLSI smart pixel technology based on GaAs/AlGaAs MQW modulators," *Int. J. Optoelectron.*, vol. 11, pp. 181–198, 1997.
- [16] J.-M. Wu, C. B. Kuznia, B. Hoanca, C.-H. Chen, and A. A. Sawchuk, "Demonstration and architectural analysis of complementary metal-oxide semiconductor/multiple-quantum-well smart-pixel array cellular logic processors for single-instruction multiple-data parallel-pipeline processing," *Appl. Opt.*, vol. 38, no. 1, pp. 2270–2281, 1999.
- [17] D. Fey, B. Kasche, C. Burkert, and O. Tschaechle, "Specification for a reconfigurable optoelectronic VLSI signal processor suitable for digital signal processing," *Appl. Opt.*, vol. 37, no. 2, pp. 284–295, 1998.
- [18] D. Fey, "Transformation of a 2-D VLSI systolic adder circuit in 3-D circuits using optical interconnections," in *EURO-PAR'96 Parallel Processing 2nd Int. Euro-Par Conf.*, vol. II, L. Bouge et al., Eds., Lyon, France, Aug. 1996, pp. 478–485.
- [19] J. van Campenhout, H. van Marck, J. Depreitere, and J. Dampre, "Optoelectronic FPGAs," *IEEE J. Select. Topics Quantum Electron.*, vol. 5, pp. 306–315, Mar./Apr. 1999.
- [20] M. Vasilko and D. Ait-Boudaoud, "Optically reconfigurable FPGAs: Is this a future trend?," in *Proc. Int. Workshop Field Programmable Logic Architectures, Smart Applications, New Paradigms and Compilers*, Darmstadt, Germany, 1996, pp. 270–279.

- [21] S. S. Sherif, S. K. Griebel, A. Au, D. Hui, T. H. Szymanski, and H. S. Hinton, "Field programmable smart pixel arrays: Design, VLSI implementation and applications," *Appl. Opt.*, vol. 37, no. 2, pp. 284–295, 1998.
- [22] H. Neefs, P. Van Heuven, and J. Van Campenhout, "Latency requirements of optical interconnects at different memory hierarchy levels of a computer system," *Proc. Optics in Computing, OC'98*, vol. 3490, pp. 552–555, June 1998.
- [23] (1997) Data Sheet INTEL Pentium Microprocessor. Intel Corp.. [Online]. Available: <ftp://download.intel.nl/design/pentium/datashts/24199710.pdf>
- [24] N. McArdle, M. Naruse, H. Toyoda, Y. Kobayashi, and M. Ishikawa, "Reconfigurable optical interconnections for parallel computing," *Proc. IEEE*, vol. 88, pp. 829–837, June 2000.
- [25] M. Ishikawa and N. McArdle, "Optically interconnected parallel computing systems," *IEEE Computer*, pp. 61–68, Feb. 1998.
- [26] G. Palm, "On associative memories," *Bio. Cybern.*, vol. 36, pp. 19–31, 1980.
- [27] H. Toyoda and M. Ishikawa, "Learning and recall algorithm for optical associative memory using a bistable light modulator," *Appl. Opt.*, vol. 34, no. 17, pp. 3145–3151, 1995.
- [28] (1997) XC6200 Field Programmable Gate Arrays. Xilinx Data Book. [Online]. Available: <http://www.xilinx.com/>
- [29] "The National Technology Roadmap for Semiconductors," Semiconductor Industry Association, Sematech, Inc., San Jose, CA, 1997.
- [30] G. Palm, "The PAN system and the WINA project," in *Euro-ARCH'93 European Congr. Computer Science*, Berlin, Germany, 1993, pp. 142–156.
- [31] H. Bartelt, F. Schrempel, L. Hoppe, and W. Wittman, "Fiber optical devices for massively parallel optoelectronic interconnects in PMMA," in *Proc. 4th National Workshop Optics in Computing (ORT'99)*, Jena, Germany, Oct. 1999, pp. 6–9.
- [32] L. Hoppe, J. M. Köhler, H. Bartelt, and B. Höfer, "Zweidimensionales Faserarray und Verfahren zu seiner Herstellung," German Patent 199 25 015 4, 1999.
- [33] S. J. Hinterlong, S. A. Novotny, and J. M. Sasian-Alvarado, "Optical fiber array and process of manufacture," U.S. Patent 5 394 498, 1995.
- [34] M. Yamane, J. Taga, and S. Yamaguchi, "Optical Fiber Array and a Method of Producing the Same," U.S. Patent 5 566 262, 1996.
- [35] K. Koyabu, T. Yamamoto, and F. Ohira, "Fabrication of two-dimensional fiber array," *NTT R&D*, vol. 45, no. 9, 1996.
- [36] M. Johnck and A. Neyer, "2D optical array interconnects using plastic optical fibers," *Electron. Lett.*, vol. 33, pp. 888–889, 1997.
- [37] M. Kuijk, D. Coppée, and R. Vounckx, "Spatially modulated light detector in CMOS integrated with sense-amplifier receiver operating at 180 Mb/s for optical data link applications and parallel optical interconnects between chips," *IEEE J. Select. Topics Quantum Electron.*, vol. 4, no. 6, pp. 1040–1045, Nov./Dec. 1998.
- [38] A. W. Lohmann, "Image formation of dilute arrays for optical information processing," *Opt. Commun.*, vol. 86, pp. 364–370, 1991.
- [39] N. Streibl, "Beam shaping with optical array generators," *J. Mod. Opt.*, vol. 36, pp. 1559–1573, 1989.
- [40] J. R. Fienup, "Phase retrieval algorithms: A comparison," *Appl. Opt.*, vol. 21, pp. 2758–2769, 1982.
- [41] M. Gruber, J. Jahns, and S. Sinzinger, "Integrated opto-electronic implementation of a binary associative memory," *Tech. Dig. MOC/GRIN'97*, pp. 86–89, 1997.
- [42] —, "Planar-integrated optical vector-matrix-multiplier," *Appl. Opt.*, to be published.



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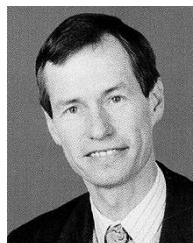


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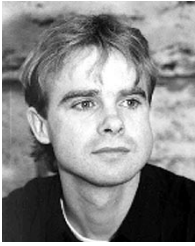
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