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Multichip module with free-space optical interconnects and VCSEL-solder-joints

C. Gimkiewicz, D. Hagedorn

Abstract The design of a multichip module with planar optical interconnects is presented. Electrical (local) interconnects for intra-chip communication and optical interconnects for chip-to-chip communication are implemented onto the same substrate of a planar-integrated free-space optical system. We suggest to integrate the optical emitter/detectors (VCSEL diodes) into solder balls; onto these solder balls IC carrying silicon chips can be flip-chip bonded like on a common ball grid array. With respect to the thermal load thermally conductive vias are incorporated into the package, too. We show that typical packaging errors can be tolerated by the optical system, which is designed for space variant interconnects and enables thin film replication techniques of temperature sensitive materials.

1 Introduction

The communication between electronic chips in a computer or in a switching system is limited by architectural, physical and topological problems, Goodman et al. (1984). Optical solutions, in particular free-space optics, for implementing massively parallel, high-bandwidth interconnections have been discussed by many authors, in McCormick (1993), for example. The use of free-space optical interconnects requires suitable hardware and architectures. Planar integrated free-space optics, or briefly planar optics, was suggested and demonstrated, Jahns (1994) gives an overview. In planar optics vertical-cavity surface-emitting laser diode (VCSEL) arrays as emitters are of interest. The emitted light beams are traveling through an optical substrate on different zigzag paths in parallel. Often fused silica is used as a substrate with a thickness of one to several millimeters. The emitter, detector and silicon chips are bonded directly onto the substrate, Fig. 1a, or onto a spacer-chip by flip-chip bonding. Optical components for the beam collimation, imaging, filtering and reflection are integrated onto the glass by means of standard lithographic processes, thin film deposition and dry etching.

Here we consider a multichip module (MCM) based on a planar optical system. Especially long interconnects are of interest to be implemented optically, because of several reasons: first the area consumption of a laser diode in an array – the typical pitch ranges from 100 μm to 250 μm – is smaller than the size of a contact pad for an *external* electrical line. Also parasitic effects and power consumption of electrical lines limit both the reduction of the line cross section and the transmission speed. Thus long electrical lines (global intra-chip lines or external inter-chip interconnects) with line length of up to several millimeters suffer from significantly slower data rates than local lines.

Three approaches for the implementation of optical interconnects can be regarded, Fig. 1. In principle the emitter-chips and the integrated circuit (IC) chips can be placed side-by-side onto the optical substrate, Fig. 1a, or in stacked groupings, Fig. 1b. For the integrated circuit (IC)-chip integration it is essential to reduce the line length between electrical and electrooptical components to benefit of the faster signal transmission and of less parasitic effects of optical interconnects. Also, the less area is consumed by the external electrical lines, the more local wiring and thermally conductive vias can be implemented. Thus the distribution of optoelectronic components among the chip area and close to the demanding ICs is prefered, Fig. 1b and c. The stacked performances require a transparent emitter-substrate or the structuring of the IC-chip, Fig. 1b.

In this paper we present the idea to integrate VCSEL diodes as optical emitters into solder joints connecting the optical substrate and the IC-chips. For the hybrid integration, Fig. 1c, the emitter substrate has to be removed. As material for the optical substrate we suggest to use fused silica; besides its high transparency at the wavelengths of interest (VIS, NIR), it obtains a low dissipation factor $\tan(\partial) = 0.0001–0.0003$ at 1 GHz, which makes it a viable substrate for electrical lines for high frequency signals thus enabling the coexistence and cofabrication of electrical (local) interconnects for intra-chip communication and optical interconnects for long interconnects; then the ICs may communicate through local electrical lines and through three-dimensional optical paths that are propagating along a zigzag-axis in the transparent substrate, Fig. 2.

Each optical interconnect may be realized by its own imaging system, which is referred to as micro-lens array

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C. Gimkiewicz*(✉), D. Hagedorn
Department of Optical Communication Technology,
University of Hagen,
Feithstr. 140-PRG, 58084 Hagen, Germany

**Present address*:
CSEM SA, Optoelectronic Devices,
Badenerstrasse 569, 8048 Zürich, Switzerland
e-mail: christiane.gimkiewicz@csem.ch

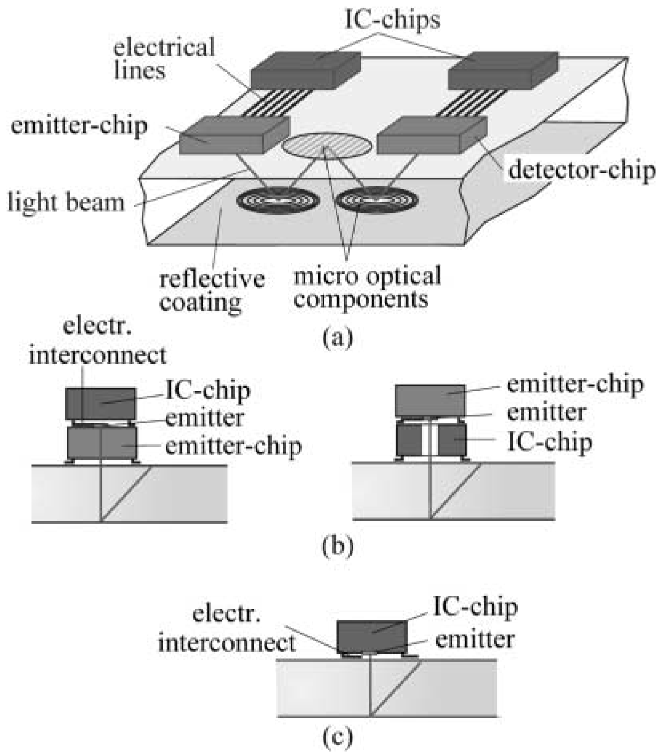

Fig. 1a–c. Chip integration with planar-integrated free-space optical interconnects **a** co-planar placement of the chips, **b** stacked chips and **c** hybrid integrated emitters

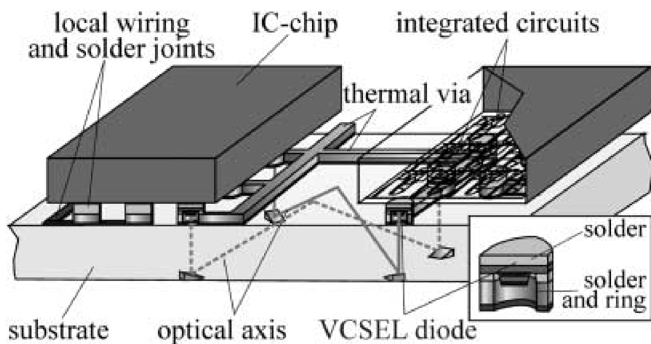

Fig. 2. A multichip module with planar integrated free-space optical interconnects. The VCSEL diodes are integrated into the solder joints between the IC-chips and the optical substrate (see enlarged section). Local electrical wiring and global optical interconnects are implemented

system or micro-channel system (McCormick, 1993). Here we use gray-tone lithography to create refractive micro-optical components. Since polymers like PMMA suffer hazardiously from temperatures above ~90 °C the photo resist structures are usually transferred into the fused silica substrate by reactive ion etching (RIE). Otherwise flip-chip bonding of the chips would cause deformations of the micro-optics. One approach to avoid long term RIE etching processes is to bond the chips onto a second chip (spacer) and to align afterwards the spacer with the bonded chips towards the optical board. The idea of an optical spacer has been suggested already by Acklin and Jahns (1994). In their packaging considerations an implemented spacer can be used as an efficient heat spreader, it may carry ICs and provides an optical spacing.

Here, we suggest to bond the active components directly onto the substrate to reduce the number of process steps. In the second section we explain the proposed integration method for the VCSEL diodes; in that context we improve their cooling by thermal vias. The micro-optical components are placed only onto the bottom of the substrate after the flip-chip bonding. We report about the limitations of such an optical design in Sect. 3; the relation-ship between the optical spacing and the beam divergence is elaborated considering optical and thermal aspects. In the 4th section we calculate packaging tolerances. In the last section we discuss the efficiency of optical interconnects for MCMs.

2
The fabrication of VCSEL-solder-joints

The integration of optoelectronic components onto electronic chips has been demonstrated by standard techniques like flip-chip bonding and substrate removal by Goossen et al. (1995). Also smart pixels based on VCSEL diodes integrated onto silicon have been demonstrated for example by Knüpfer et al. (1997). Here we suggest the integration of the laser diodes onto the optical substrate with equivalent techniques to achieve solder bumps on top of the laser diodes, which are later on the acceptors for the direct chip attachment. In Fig. 2, a VCSEL diode integrated into the solder bump is shown. VCSEL diodes in principle consists of epitaxially grown distributed Bragg reflectors (DBR) surrounding an active layer. The mirror layers are n- or p-doped, about twenty layers are stacked to receive the necessary reflectivity for the short laser diode cavity. The active region contains one or more quantum wells. Because of the sandwiched position between the low thermally conductive glass and the silicon chip, and especially when the VCSEL diodes are placed with a minimum pitch of about one hundred microns, the application of high efficient VCSEL diodes with oxid confined apertures, (Huffaker et al., 1994), may improve the systems performance.

In our design the laser diodes are bonded for electrical, mechanical, and for thermal purposes, too, because the heat is transfered to outer regions through thermally high conductive vias as suggested in (Gimkiewicz and Jahns, 1998). Therefore we have electroplated horizontal metal stripes with doughnut shaped tips for each VCSEL onto the substrate. The electroplated ring encloses each diode while bonding, it protects the facet from underfillers and reduces the thermal and ohmic resistance between the VCSEL diodes and the metal stripes, (Gimkiewicz and Hagedorn, 2000). We have fabricated such silver stripes and rings with a height of up to 25 μm. Indium, 3 μm thick, can be used as solder.

To integrate the diodes into these solder rings, the following process steps are necessary, see Fig. 3. First, deep trenches have to be etched into the epitaxially grown structures on the Galliumarsenide (GaAs)-substrate to isolate the VCSELs, Fig. 3a. Such trench etches have been performed for wafer bonding of diodes on hybrid substrates, Choquette et al. (1998). Here we suggest to use

VCSELs grown on p+-substrates, although the common p-dopants like beryllium or zinc may diffuse into the active layer while the epitaxy. Lear et al. (1997) have demonstrated VCSEL diodes on p+-substrates with carbon as dopant, which is less diffusive. In general the p-doped DBR obtains a higher ohmic and thermal resistivity than the n-doped DBR. Due to the higher resistivity of the p-doped mirror, the structure benefits when the p-mirror area is enlarged and the smaller top-mirror is n-doped. Lear's diodes have shown a higher efficiency than comparable n+-grown devices.

After the definition of the VCSEL diodes the GaAs-chip is flip-chip bonded onto the electroplated thermal vias, Fig. 3b, and underfilled by an epoxy, Fig. 3c. The underfiller reduces the stress in the solder joints, it increases the heat dissipation and the stability of the bond, too. Since the ring contacts are protecting the laser facets, thermally conductive adhesives, e.g. with diamond particles, can be injected without harming the light path.

Subsequently the substrate is removed, Fig. 3d; Goossen et al. (1995) have used jet etching for the substrate removal. As etch stop layer one may profit from the higher etch resistivity of the mirror layers. After a photolithographic step has defined solder bumps on top of each diode, with thin film deposition and lift-off techniques as well as with electroplating one can achieve solder pads on the VCSEL's backside, Fig. 3e. This 2D-array of solder pads may look similar to a ball grid array. An IC-chip is flip-chip bonded onto the buried VCSELs like on a solder ball grid array, Fig. 3f. A critical task is the second bonding step: the melting of the previously fabricated solder bonds has to be avoided. Thin indium layers may transform completely to intermetallic silver-indium layers with higher melting point. For example a fluxless bonding technique may result in $AuIn_2$ with a melting point at 166 °C (Chen, 1997). A gold layer may ensure the formation of $AuIn_2$ melting at 541 °C. Otherwise the solder heating through the IC-chip is necessary, and a low melting solder like Indium (melting point at $T_m = 155$ °C) may be suitable.

3
The micro-channel system

The micro-channel system provides each laser source in a 2D-array its own micro-lens system, Fig. 4a. Figure 4b depicts the folded layout for a planar micro-channel system with two reflective lenses. This micro-channel system allows an individual design for each light path, it is called space variant.

The deflection angle is typical on the order of $\alpha = 5°–20°$. For long interconnects one has to consider that each reflection at a reflective surface causes losses of up to several percent, when simple metallic mirror layers like aluminum are used. The larger the deflection angle the lower is the total number of reflections and the more efficient is the system. To create high deflection angles we have investigated diffractive components, micro-prisms and reflective coated prism structures. Prisms are preferred to diffractive elements, since phase gratings as coupling elements show a trade-off between deflection angle and coupling efficiency. Refractive components however provide deflection angles depending on the refractive index of the substrate. In GaAs its high refractive index allows deflection angles of up to $\alpha = 40°$, but in

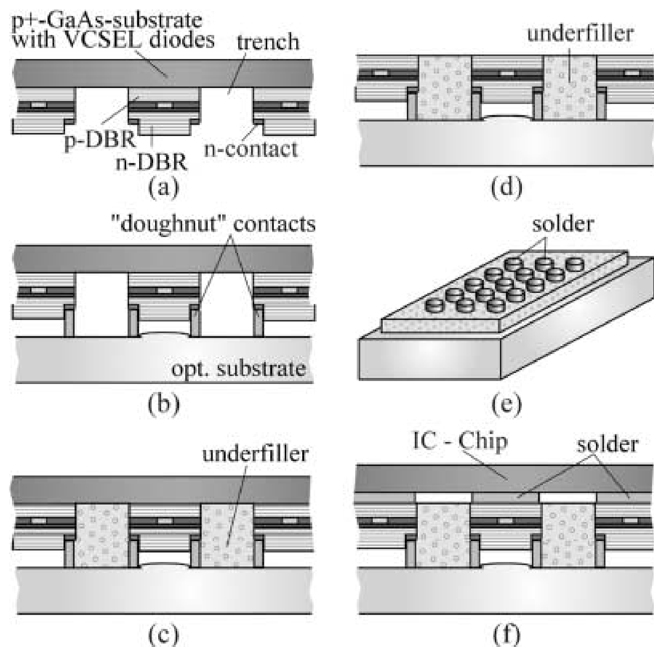

Fig. 3a–f. Integration of the VCSEL diodes in a MCM with optical interconnections: **a** trench etching of the GaAs-chip to define the VCSELs, **b** flip-chip bonding onto the optical substrate with doughnut shaped bumps, **c** underfilling, **d** removal of the GaAs-substrate, **e** metallization of the backside of the VCSEL diode, and **f** IC-chip bonding

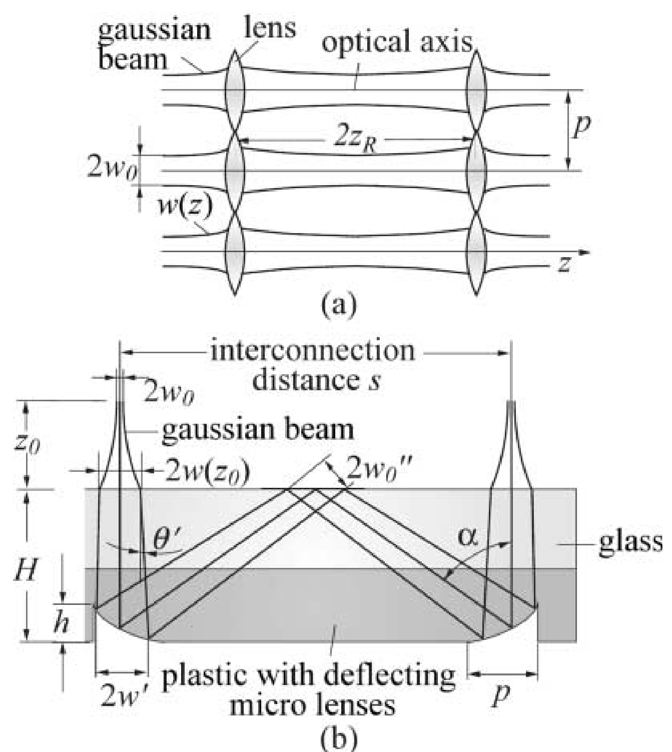

Fig. 4a, b. A micro-channel system **a** in principle, **b** implemented with deflective components in PMMA

fused silica and for the same prism sag the angle is below 10°, Gimkiewicz et al. (1998). Reflective micro-prisms enable high deflection angles without a material dependency. Such micro-prisms were fabricated in thick photoresist by analog lithography with an e-beam written gray tone mask of high energy beam sensitive (HEBS) glass. The HEBS mask can be used in a standard mask aligner. The sag h of the prisms or lenses and p, the lateral size, determine the deflection angle $\alpha = 2\arctan(h/p)$. We obtained prism sags of up to $h = 20$ μm in photoresist corresponding to a deflection angle of up to $\alpha = 22.6°$. After the development of the resist the analog profile can be etched into quartz glass by reactive ion etching. Apparently this technique can be applied to create prisms or spherical profiles.

The integration technique of the emitter determines the optical spacing z_0. In the previous section the hybrid integration of the VCSEL diode has been described in detail. Here we regard the thickness of the solder joints, i.e. the spacing z_0 between the laser diode and the optical substrate. The spacing z_0 influences the optical systems design, and z_0 has to be balanced accounting for three parameters: the minimum feature size of the solder joint technology, the beam divergence of the laser diode and the spacing required for cooling. The spacing z_0 given by the minimum feature size of the solder joints can be estimated by the diode pitch p and the emission window with the diameter $2w_0$:

$$z_0 < ad \tag{3.1}$$

wherein a defines the aspect ratio (line thickness over line width) and $d \approx (p - 2w_0)/4$ is the minimum width of the solder ring. Typical values are $a = 1$–2, $p = 100$ μm, $z_0 < 40$ μm to enable fine line structures. We suggest to neglect coupling lenses and to place all optical components on the bottom side of the substrate, where they are not involved into bonding processes and do not need to be etched into temperature stable material. In mass fabrication the optics may be imprinted or jetted directly onto the quartz substrate. Gale et al. (1994) have demonstrated another suitable technique: the UV-embossing of thin film optics on glass. Also, substrates replicated by injection molding or hot embossing can be bonded adhesively as a complete optical system onto the glass, Fig. 4b.

To model the beam propagation in a planar optical system with VCSEL diodes a Gaussian beam model can be applied. A Gaussian beam shows a rotational symmetric intensity distribution $I(r)$ in accordance to the Gauss function. At a so-called Gaussian radius w the beam intensity has decreased to a value $1/e^2$ of the central intensity $I(0)$. Along the propagational axis z the beam radius $w(z)$ may change, Fig. 4. In a planar optical system for example, Fig. 4b, the beam radius changes from the initial beam waiste w_0 at the laser facet to a radius $w(z_0)$ on the optical substrate, which can be calculated by

$$w(z_0) = w_0\sqrt{1 + \left(\frac{z_0}{z_R}\right)^2} \tag{3.2}$$

with the Rayleigh range $z_R = \pi w_0^2/\lambda$ for a wavelength λ.

In the substrate with refractive index n the beam diverges to a value $w'(z')$, Fig. 4b.

$$w'(z') = w'_0\sqrt{1 + \left(\frac{z'}{z_{R,n}}\right)^2} \tag{3.3}$$

(Here $z_{R,n} = \pi w_0'^2 n/\lambda$ denotes the Rayleigh range in the medium.) The Gaussian beam has travelled approximately a total optical distance $z' \approx nz_0 + H - h/2$. The beam in the medium corresponds to a virtual beam waiste w'_0, which can be calculated with the help of Snell's law and the divergence angle $\theta' = \arctan(\partial w'/\partial z')$ to

$$w'_0 = \frac{w(z_0)}{\sqrt{1 + \left[\pi w(z_0)\tan(\theta')\frac{n}{\lambda}\right]^2}} \tag{3.4}$$

At the bottom of the substrate the micro-optic extends to a maximum size similar to the diodes pitch p. The beam spot should not exceed a fraction of p to avoid diffraction at the edges of the micro-optics:

$$2w'(z') = p/k < p \tag{3.5}$$

A factor $k = 1.6$ reduces the power loss by the limited lens size below 1%, and diffraction effects become negligible (Belland and Crenn, 1982).

After deflection from the lens, the Gaussian beam receives a new beam waiste w''_0. The optimum beam waiste w''_0 of the folded beam in the glass is approximately

$$w''_0 = w'/[\sqrt{2}\cos(\alpha)] \ ,$$

compare Sauer et al. (1994). The Rayleigh range of the reflected beam determines the maximum interconnection length s_{max}:

$$s_{max} = 2w_0''^2 \pi n \sin(\alpha)/\lambda \tag{3.6}$$

For small laser diameters, i.e. $w_0 \ll p/(2k)$, the substrate thickness H and hence the total interconnection length s, are limited by the beam divergence (see Eq. (3.5)):

$$s_{max} = 2(H - h/2)\tan(\alpha) \tag{3.7}$$

Assuming a spacing as given by Eq. (3.1) the interconnection distance s depends on the beam waiste w_0, the curves are plotted in Fig. 5 for the Rayleigh range condition (Eq. (3.6)) as well as for the Gaussian beam divergence (Eq. (3.5)). For the considered Gaussian radii w_0 and the corresponding beam divergence (Eq. (3.5)) the substrate thickness varies between $H = 310$ μm for a diameter of $2w_0 = 4$ μm and up to $H = 2643$ μm for $2w_0 = 40$ μm.

The third parameter with an influence on the spacing is the heat dissipation of the VCSEL diodes, which are bonded onto the heat spreading vias with doughnut shaped tips. With increasing thickness of the thermal via or heat spreading layer the thermal resistance R_{th} is reduced. Nakwaski and Osinski (1992) suggested a simple formula for the thermal resistance of VCSEL diodes on a substrate: the sum of the substrate's resistance and the spreading resistance. Here we assume as substrate the heat spreading thermal vias – that are metal stripes of length l_{via}, thickness z_0 and width d, and

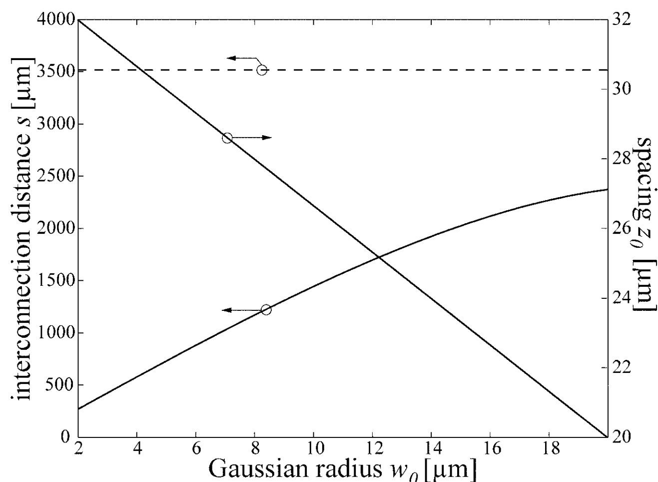

Fig. 5. Calculated spacing z_0 and interconnection distance s limited by the beam divergence for different beam waistes w_0 and with $k = 1.6$, $a = 4/3$, $\lambda = 850$ nm, $n = 1.5$, $p = 100$ µm and $h = 21.5$ µm ($\alpha = 20°$). The substrate thickness H is derived for a spot radius $w' = p/(2k)$ at the bottom of the substrate. The dashed line indicates the maximum interconnection distance by the Rayleigh condition formulated in Eq. (3.6)

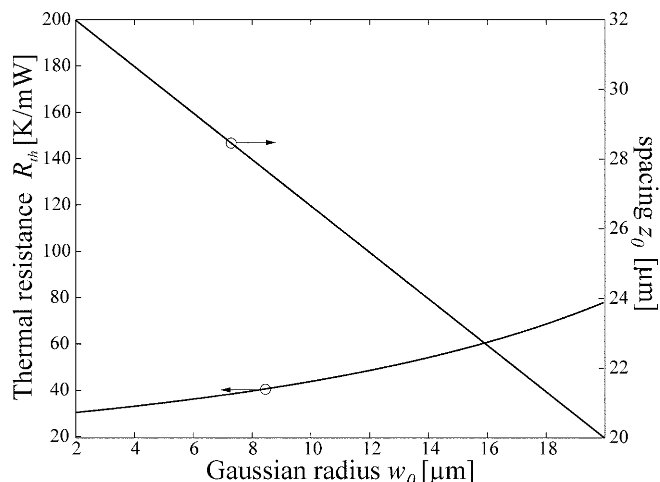

Fig. 6. Calculated thermal resistance for different laser dimensions and assuming a VCSEL diode bonded onto a silver via ($\kappa_2 = 4.29$ W cm^{-1} K^{-1}) with length $l_{via} = 10$ mm and solder bonds with an aspect ratio $a = 4/3$

with a thermal conductivity κ_2 – guiding the heat to marginal regions.

$$R_{th} \approx R_{th,s} + \frac{l_{via}}{\kappa_2 z_0 d} \tag{3.8}$$

The spreading resistance of the interface $R_{th,s}$ can be estimated by (see Cooper et al., 1969):

$$R_{th,s} \approx \frac{(1 - d'/p)^{3/2}}{2\kappa d'} \tag{3.9}$$

with the thermal conductivity of the interface $\kappa = 2\kappa_1\kappa_2/(\kappa_1 + \kappa_2)$. The emission window with a diameter $2w_0$ is not in contact with the doughnut shaped ring contact. Thus the contact area is determined by the minimum feature size d of the ring contact, it is here approximated with $d'^2 = 8w_0 d + 4d^2$. Assumptions to estimate a viable heat spreader thickness may include a diode pitch of $p = 100$ µm, that are 10,000 devices per square centimeter, and an arbitrary thermal power dissipation of 25 W/cm^2. For the densely packed VCSEL diodes the thermal load per diode may not exceed $P_{th} = 250$ µW in the pulsed mode. (One may note that a heat density of 25 W/cm^2 is dissipated by only $N = 1000$ electrical lines on a square centimeter with a line length of $l = 100$ µm, an assumed voltage drop of $U = 0.8$ V, a frequency $f = 1$ GHz and a capacitance of $C' = 0.4$ pF/mm according to $P = NC'fU^2l$.)

The temperature increase ΔT in each diode is limited to gain a certain life-time and reliability. Junction temperatures in ICs are in the order of $T = 100$ °C, for the VCSEL diodes we consider a temperature increase of $\Delta T = 50$ °C. To ensure the low temperature increase the thermal resistance of the thermal vias may not exceed

$$R_{th} = \Delta T / P_{th} = 200\,\mathrm{K/mW} \tag{3.10}$$

Considering the Eqs. (3.8), (3.9) and (3.10) for the VCSEL material GaAs ($\kappa_1 = 0.44$ W cm^{-1} K^{-1}) and silver as via material ($\kappa_2 = 4.29$ W cm^{-1} K^{-1}) one may obtain another value range of suitable spacer thicknesses z_0. Figure 6 shows a plot of the thermal resistance in dependency of the laser diameter $2w_0$. Within a diode array of a fixed pitch p the contact area is decreasing with increasing emission window. Naturally the thermal resistance is growing, too. As can be deduced from Fig. 6 for all calculated spacer thicknesses, the thermal resistance from equation (3.8) is below the set limit of about 200 K/mW. The result indicates even for large emission windows and lower thermal conductivities a suitable spacing within $20\ \mu\mathrm{m} < z_0 < 32\ \mu\mathrm{m}$. The presented, simple calculation has neglected soldering effects, which may reduce the thermal conductivity of the vias, and the fact, that electroplated metals show usually a reduced thermal conductivity due to a lower density and impurities.

4
Packaging tolerances

We have worked with a Gaussian beam tracing program to elaborate on the limits of the alignment errors while flip-chip bonding of the VCSEL diodes into the doughnut shaped solder rings. The investigated errors are: a lateral shift of the VCSEL, a varying spacing between the VCSEL diode and the optical substrate, and a tilting of the chip. The tolerances are calculated through the overall efficiency. We have assumed a detector diameter of $D = 2kw_0$, ideal reflective coatings ($R = 1$) and ideal transmission ($T = 1$). The efficiency per lens η_{lens} – that is the fraction of the light power reflected from the optical components – is given as the integral of the Gaussian intensity distribution over the lens area. The overall efficiency is the product of the single efficiencies. The range of fabrication errors, that can be simulated with the Gaussian ray tracing program, is limited by the lens size: If a beam trace with a diameter $2w$ is not completely onto the considered optical component, diffraction and scattering effects will occur. In that case the Gaussian beam model and the calculated beam traces are no longer valid. Maximum

Table 1. Fabrication errors and their effect onto the system's overall efficiency η

No alignment error	$\eta = 0.9505$
Lateral shift: $-3\mu m < x < 0.5\ \mu m$	$0.9212 > \eta > 0.9252$
Spacing: $40 < z_0 < 20\ \mu m$	$0.9085 > \eta > 0.9733$
Tilt angle: $-1.8° < \delta < 0.4°$	$0.9213 > \eta > 0.9101$

calculable tolerances and the corresponding overall efficiency are given in Table 1. The values are based on a laser diameter of $2w_0 = 10\ \mu m$ and a lens size $p = 100\ \mu m$, which determines a substrate thickness of $H \leq 819\ \mu m$. With these data and for a lens depth of $h = 21.5\ \mu m$, a wavelength $\lambda = 850$ nm, and a spacing of $z_0 = 30\ \mu m$ the maximum interconnection distance s is 732 μm.

The results in Table 1 show the unsymmetry of tolerated bonding errors: the smaller the spacing, for example, the higher the efficiency, because the less the Gaussian beam has broadened, before it reaches the optical substrate. Thus, the better it is refocused into the detector. Also, the lateral shift on the lenses causes a larger error in the deflection angle, if the displacement points outwards of the system; the beam deviates from the central point of the lenses and towards steeper, more deflecting parts. The same reason explains the difference in the considered tilt angles and the corresponding efficiency. Since flip-chip bonding shows a lateral displacement in the order of 1 μm to 2 μm, it is necessary to consider in an improved design the unsymmetric packaging tolerances of the system. However, the calculated range is sufficient for flip-chip bonding.

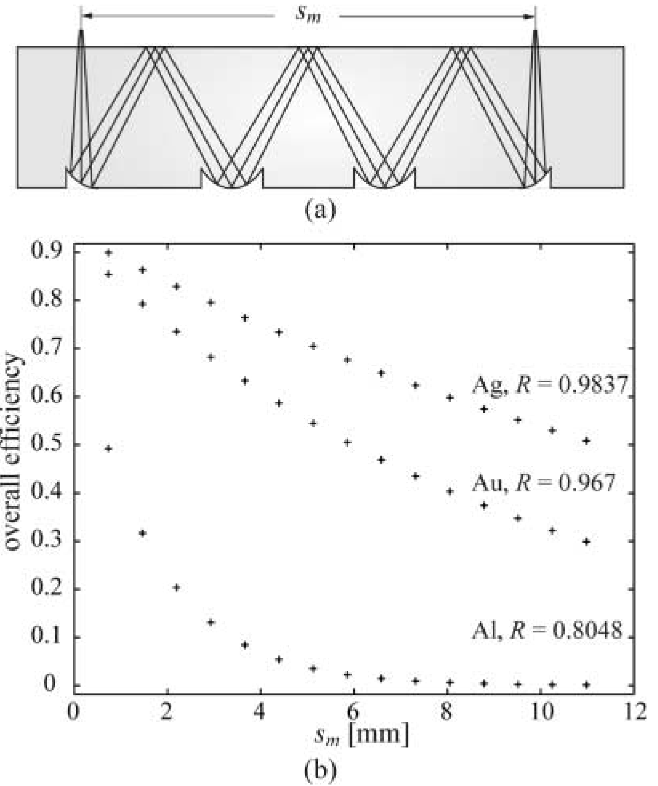

Fig. 7. **a** Principle of a lens wave guide, $m = 3$, and **b** the overall systems efficiency for long interconnection distances $s_m = ms_{max}$, $s_{max} = 732\ \mu m$, $\eta_r = R$ as indicated and $\eta_{lens} = 0.9922$; $\eta_{in} = 0.96$ and η_{out} is neglected here

5 Discussion of long distance interconnects

So far, we have presented the packaging of a MCM with optical interconnections based onto the integration of VCSEL diodes into ring-shaped solder joints. The fabrication errors and the resulting efficiencies imply that the system can tolerate errors of a standard flip-chip bonding process and also matches inaccurate spacing, e.g. inaccurate heights of the electroplated heat conductive stripes and the deposited solder. For interconnects with $s > s_{max}$ systems with multiple length of s_{max} can be performed by relaying the beam in a lens waveguide, Fig. 7a: the central lens does not change the beam's deflection but focuses it towards the next lens. The overall efficiency for the distance $s_m = ms_{max}$ can be calculated to:

$$\eta = \eta_{in}(\eta_r)^{2m+1}(\eta_{lens})^{m+1}\eta_{out} \quad (5.1)$$

Here, η_{in} and η_{out} represent the effect of the input and output reflection losses, η_r is the reflectivity of the mirror coatings; it is on the order of $\eta_r = R = 0.8048$ for aluminum ($\lambda = 850$ nm), $R = 0.9837$ for silver or $R = 0.967$ for gold used instead. When no alignment error occurs, the loss per optical component η_{lens} is only $\eta_{lens} = 0.9922$. For $s_{max} = 732\ \mu m$, the system's efficiency is depicted in Fig. 7b.

For silver mirrors an efficiency around 40% for interconnection distances of up to 10 millimeters has been achieved. Amplifier circuits may be necessary, especially for bidirectional optical bus systems based on VCSEL diodes as emitters and detectors. However, the presented module is feasible and obtains several advantages: because fused silica is proposed as substrate material local electrical lines for high speed intra-chip communication directly on the glass seem to be viable. Standard flip-chip bonding of the VCSEL diodes and of the silicon chips can be used, as indicated by the alignment tolerances and because the optical components are separated from the bonded electrical contacts by the glass substrate. The integration of VCSEL diodes into solder joints allows a direct chip attachment. The optical system is easy to package, since the lenses can be obtained by lowcost technologies and still high deflection angles can be fabricated. Although metallic mirrors have the advantage of low chromatic dispersion, a further improvement may incorporate dielectric layers with a high reflectivity $R > 0.99$, since Fig. 4b shows the determining effect of the reflectivity on the overall efficiency.

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